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PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,931	JENG, ERIK S.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,13-21,25-27,29,37-48 and 53-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *53-82* is/are allowed.

6)☒ Claim(s) *1-3, 5, 13-21, 25-27, 29, 27-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bae et al. (US 2003/0094662 A1).

In re claim 1, Bae (Fig. 8) discloses a semiconductor device, comprising:

A semiconductor substrate (100);

A gate oxide (115) formed on said semiconductor substrate;

A gate structure (140) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

An isolation layer (155) formed over the sidewall of the gate structure and said substrate;

First spacers (175) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a

spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;.

Source and drain regions (200, 205, 160) formed adjacent to said gate structure and under said undercut structure; and

Silicide (215, 210) formed on said gate structure and said source drain regions.

In re claim 13, Bae discloses the device of claim 1, wherein said isolation layer is formed of an oxide (section [0047]).

In re claim 14, Bae discloses the device of claim 1, wherein said first spacers are formed of nitride (section [0041]).

In re claim 15, Bae discloses the device of claim 1, wherein said silicide material includes $TiSi_2$, $CoSi_2$ and NiSi (section [0053]).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 13-21, 25-27 and 37-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. (U.S. Patent No. 6,482,691 B2) in view of Tsai et al. (U.S. Patent No. 6,613,623 B1).

In re claim 1, Wu (Figs. 13, 15) discloses a semiconductor device, comprising:

A semiconductor substrate (22);

A gate oxide (54) formed on said semiconductor substrate;

A gate structure (56) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

An isolation layer (40) formed over (covering a portion of) the sidewall of the gate structure;

First spacers (46) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (62, 64) formed adjacent to said gate structure and under said undercut structure; and

Silicide (56) formed on said gate structure.

Wu does not expressly disclose silicide formed on the source/drain regions. Tsai et al. (Figs. 1-6) discloses a gate undercut structure with silicide (26, 28) covering the source/drain regions. It would have been obvious for one skilled in the art at the time of the invention to form

silicide regions as disclosed by Tsai on the source/drain regions of Wu for the purpose, for example, of enhancing the speed of the semiconductor device.

In re claim 2, Wu in view of Tsai discloses the device of claim 1, further comprising pocket ion implantation regions (70, 72) located adjacent to said source and drain regions and under said undercut structure, wherein the conductivity type of the pocket ion implantation region is opposite to the one of the source and drain regions (Wu; column 5, lines 20-22 and 35-38).

In re claim 3, Wu in view of Tsai discloses the device of claim 1, further comprising lightly doped drain regions (66, 68) adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than on the one of said source and drain regions and said lightly toped drain regions is closer to the channel under said gate structure than said source and drain regions; and

Pocket ion implantation regions (70, 72) adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions (Wu; column 5, lines 20-22 and 35-38).

In re claim 13, Wu in view of Tsai discloses the device of claim 1, wherein said isolation layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 14, Wu in view of Tsai discloses the device of claim 1, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 15, Wu in view of Tsai discloses the device of claim 1, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 16, Wu in view of Tsai discloses the device of claim 1, wherein said isolation layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 17, Wu in view of Tsai discloses the device of claim 1, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 18, Wu in view of Tsai discloses the device of claim 1, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 19, Wu in view of Tsai discloses the device of claim 1, wherein said isolation layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 20, Wu in view of Tsai discloses the device of claim 1, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 21, Wu in view of Tsai discloses the device of claim 1, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 25, Wu (Figs. 13, 15) discloses a semiconductor device, comprising:

A semiconductor substrate (22);

A gate oxide (54) formed on said semiconductor substrate;

A gate structure (56) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

A second dielectric layer (40) formed over (covering a portion of) the sidewall of the gate structure and substrate;

First spacers (46) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (62, 64) formed adjacent to said gate structure and under said undercut structure; and

Silicide (56) formed on said gate structure.

Wu does not expressly disclose silicide formed on the source/drain regions nor a dielectric layer covering the gate silicide layer. Tsai et al. (Figs. 1-6) discloses a gate undercut structure with silicide (26, 28) covering the source/drain regions and a dielectric layer (36) atop the gate silicide layer. It would have been obvious for one skilled in the art at the time of the invention to form silicide regions as disclosed by Tsai on the source/drain regions of Wu for the purpose, for example, of enhancing the speed of the semiconductor device; and it also would have been obvious to one skilled in the art at the time of the invention to form a dielectric layer as disclosed by Tsai atop the silicide layer of Wu for the purpose, for example, of providing a barrier layer to enhance separation between an upper gate connection scheme and lower peripheral insulation layers.

In re claim 26, Wu in view of Tsai discloses the device of claim 25, further comprising pocket ion implantation regions (70, 72) located adjacent to said source and drain regions and under said undercut structure, wherein the conductivity type of the pocket ion implantation

region is opposite to the one of the source and drain regions (Wu; column 5, lines 20-22 and 35-38).

In re claim 27, Wu in view of Tsai discloses the device of claim 25, further comprising lightly doped drain regions (66, 68) adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than on the one of said source and drain regions and said lightly toped drain regions is closer to the channel under said gate structure than said source and drain regions; and

Pocket ion implantation regions (70, 72) adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions (Wu; column 5, lines 20-22 and 35-38).

In re claim 37, Wu in view of Tsai discloses the device of claim 25, wherein said isolation layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 38, Wu in view of Tsai discloses the device of claim 25, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 39, Wu in view of Tsai discloses the device of claim 25, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 40, Wu in view of Tsai discloses the device of claim 25, wherein the first dielectric layer comprises a nitride.

In re claim 41, Wu in view of Tsai discloses the device of claim 26, wherein said second dielectric layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 42, Wu in view of Tsai discloses the device of claim 26, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 43, Wu in view of Tsai discloses the device of claim 26, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 44, Wu in view of Tsai discloses the device of claim 26, wherein first dielectric layer is a nitride.

In re claim 45, Wu in view of Tsai discloses the device of claim 27, wherein said second dielectric layer (40) is formed of oxide (Wu; column 4, line 25).

In re claim 46, Wu in view of Tsai discloses the device of claim 27, wherein said first spacers are formed of nitride (Wu; column 4, lines 26-27).

In re claim 47, Wu in view of Tsai discloses the device of claim 27, wherein said silicide material includes $TiSi_2$ and $CoSi_2$ (Tsai; column 2, lines 46-47).

In re claim 48, Wu in view of Tsai discloses the device of claim 27, wherein first dielectric layer is a nitride.

4. Claims 1, 5, 9, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi et al. (U.S. Patent No. 5,734,185) in view of Tsai et al. (U.S. Patent No. 6,613,623 B1).

In re claim 1, Iguchi (Fig. 1a) discloses a semiconductor device, comprising:

A semiconductor substrate (1);

A gate oxide (17) formed on said semiconductor substrate;

A gate structure (19) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a

function, do not differentiate the claimed composition of these elements from those known to prior art;

An isolation layer (16, combination of layers) formed over (covering a portion of) the sidewall of the gate structure and said substrate;

First spacers (16, combination of layers) formed on the sidewall of said isolation layer and filled into said undercut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (31) formed adjacent to said gate structure and under said undercut structure.

Iguchi does not expressly disclose silicide layers atop the gate, source and drain regions. Tsai et al. (Fig. 6) discloses the use of silicide regions (26, 28, 30) in combination with source, drain and gate regions. It would have been obvious for one skilled in the art at the time of the invention to use silicide layers as disclosed by Tsai atop the source, drain and gate layers of Iguchi for the purpose, for example, of increasing the speed of the semiconductor device.

In re claim 5, Iguchi in view of Tsai discloses the device of claim 1, wherein the undercut-filling material filled into said undercut structure includes nitride (3) and said spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide (16a).

In re claim 9, Iguchi in view of Tsai discloses the device of claim 1, further comprising second spacers (16a) attached on said first spacers (3), wherein said second spacers are formed of oxide.

In re claim 25, Iguchi (Fig. 1a) discloses a semiconductor device, comprising:

A semiconductor substrate (1);

A gate oxide (17) formed on said semiconductor substrate;

A gate structure (19) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

A second dielectric layer (16, combination of layers) formed over (covering a portion of) the sidewall of the gate structure and substrate;

First spacers (16, combination of layers) formed on the sidewall of said isolation layer and filled into said undercut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (31) formed adjacent to said gate structure and under said undercut structure.

Iguchi does not expressly disclose silicide formed on the source/drain regions nor a dielectric layer covering the gate silicide layer. Tsai et al. (Figs. 1-6) discloses a gate undercut structure with silicide (26, 28) covering the source/drain regions and a dielectric layer (36) atop the gate silicide layer. It would have been obvious for one skilled in the art at the time of the invention to form silicide regions as disclosed by Tsai on the source/drain regions of Iguchi for the purpose, for example, of enhancing the speed of the semiconductor device; and it also would have been obvious to one skilled in the art at the time of the invention to form a dielectric layer as disclosed by Tsai atop the silicide layer of Iguchi for the purpose, for example, of providing a barrier layer to enhance separation between an upper gate connection scheme and lower peripheral insulation layers.

In re claim 29, Iguchi in view of Tsai discloses the device of claim 25, wherein the undercut-filling material filled into said undercut structure includes nitride (3) and said spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide (16a).

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al. (US 2002/0142523 A1) in view of Tsai et al. (U.S. Patent No. 6,613,623 B1)

In re claim 1, Ryu (Fig. 6) discloses a semiconductor device, comprising:

A semiconductor substrate (100);

A gate oxide (211) formed on said semiconductor substrate;

A gate structure (212) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the

claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

An isolation layer (220) formed over the sidewall of the gate structure and said substrate;

First spacers (213) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (206) formed adjacent to said gate structure and under said undercut structure.

Ryu does not expressly disclose silicide layers atop the gate, source and drain regions. Tsai et al. (Fig. 6) discloses the use of silicide regions (26, 28, 30) in combination with source, drain and gate regions. It would have been obvious for one skilled in the art at the time of the invention to use silicide layers as disclosed by Tsai atop the source, drain and gate layers of Ryu for the purpose, for example, of increasing the speed of the semiconductor device.

3. Claims 1, 5, 25 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chatterjee et al. (U.S. Patent No. 6,180,978 B1) in view of Tsai et al. (U.S. Patent No. 6,613,623 B1).

In re claim 1, Chatterjee (Fig. 8c) discloses a semiconductor device, comprising:

A semiconductor substrate (32);

A gate oxide (91) formed on said semiconductor substrate;

A gate structure (92) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

An isolation layer (74) formed over the sidewall of the gate structure and said substrate;

First spacers (82) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (96, 98) formed adjacent to said gate structure and under said undercut structure.

Chatterjee does not expressly disclose silicide layers atop the gate, source and drain regions. Tsai et al. (Fig. 6) discloses the use of silicide regions (26, 28, 30) in combination with source, drain and gate regions. It would have been obvious for one skilled in the art at the time of the invention to use silicide layers as disclosed by Tsai atop the source, drain and gate layers of Chatterjee for the purpose, for example, of increasing the speed of the semiconductor device.

In re claim 5, Chatterjee in view of Tsai discloses the device of claim 1, wherein the undercut-filling material filled into said undercut structure includes nitride (Chatterjee; column 7, line 13) and said spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide (Chatterjee; column 7, line 44).

In re claim 25, Chatterjee (Fig. 8c) discloses a semiconductor device, comprising:

A semiconductor substrate (32);

A gate oxide (91) formed on said semiconductor substrate;

A gate structure (92) formed on said gate oxide, wherein said gate structure includes an undercut structure. The limitation, "for storing carriers," is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art;

A second dielectric layer (74) formed over the sidewall of the gate structure;

First spacers (82) formed on the sidewall of said isolation layer and filled into said under cut structure. The limitation, "for storing carriers" is a recitation of the intended use of the claimed device and is not given patentable weight in this claim. The claimed structure of a spacer layer is anticipated by the prior art. If the spacer layer has a specific function, or is comprised of a particular material that exhibits a certain function, such must be claimed to differentiate the layer from that known to prior art;

Source and drain regions (96, 98) formed adjacent to said gate structure and under said undercut structure.

Chatterjee does not expressly disclose silicide formed on the source/drain regions nor a dielectric layer covering the gate silicide layer. Tsai et al. (Figs. 1-6) discloses a gate undercut structure with silicide (26, 28) covering the source/drain regions and a dielectric layer (36) atop the gate silicide layer. It would have been obvious for one skilled in the art at the time of the invention to form silicide regions as disclosed by Tsai on the source/drain regions of Chatterjee for the purpose, for example, of enhancing the speed of the semiconductor device; and it also would have been obvious to one skilled in the art at the time of the invention to form a dielectric layer as disclosed by Tsai atop the silicide layer of Chatterjee for the purpose, for example, of providing a barrier layer to enhance separation between an upper gate connection scheme and lower peripheral insulation layers.

In re claim 29, Chatterjee in view of Tsai discloses the device of claim 25, wherein the undercut-filling material filled into said undercut structure includes nitride (Chatterjee; column 7, line 13) and said spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide (Chatterjee; column 7, line 44).

Allowable Subject Matter

4. Claims 53-82 are allowed.

Response to Arguments

5. Applicant's arguments filed 06/24/04 have been fully considered but they are not persuasive.

6. In response to applicant's argument that the cited references are not non-volatile memories, (NVMs), a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Because the claim limitations match up on a one-to-one basis with the elements of the prior art, the prior art meets the claims.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800